MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

(UGC-AUTONOMOUS INSTITUTION)
Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi
NAAC Accredited with A+ Grade, NIRF India Rankings 2025 - Band: 201-300 (Engg.)
NBA Accredited - B.Tech. (CIVIL, CSE,CST, ECE, EEE, MECH), MBA & MCA
www.mits.ac.in

Examination Branch

M. Tech (VLSI Design & ES) – I Year I Semester (R24) Supplementary End Semester Examinations, December-2025

(For 2024 Admitted batch)

TIME TABLE

Academic Year: 2025– 26

Time: 10:00 AM to 01:00 PM **Duration: 3 hours**

DATE / DAY	Course Name & Code
30.12.2025 (Tuesday)	CMOS Digital IC Design- 24VESP101
31.12.2025 (Wednesday)	Microcontrollers and Programmable Digital Signal Processors- 24VESP102
01.01.2026 (Thursday)	FPGA Architectures and Applications-24VESP403
02.01.2026 (Friday)	Low Power VLSI Design-24VESP404
03.01.2026 (Saturday)	Research Methodology and IPR-24RMP101

Note: (i) Any clashes or omissions in the time table may please be informed to the Controller of Examinations Immediately.
(ii) Even if Government declares holiday on any of the above dates, the examination shall be conducted as usual.

CONTROLLER OF EXAMINATIONS

PRINCIPAL

Principal
Madanapalle Institute of
Technology & Science
MADANAPALLE

Date: 05.12.2025
Copy to:

1. ECE HOD
2. Transport Incharge
3. Notice Board (AS & Dept)
4. File (AS)